REMARKS

Claims 1-23 are pending in the application.

Claims 1-23 have been rejected.

Claims 6-7 and 17-18 have been canceled, without prejudice.

Claims 1, 5, 8, 12, 16, 19 and 23 have been amended, as set forth herein.

New Claims 24-31 have been added.

I. REJECTION UNDER 35 U.S.C. § 102

Claims 1-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by Uya (US 4,682,303). The rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Applicant has amended independent Claims 1 and 12 to recite a second adder cell operable to receive data bits, A_{X+1} and B_{X+1}, and the first and second conditional carry-out bits $C_X(1)$ and $C_X(0)$, and generate both a first conditional carry-out bit, $C_{X+1}(1)$, and a second conditional carry-out bit, $C_{X+1}(0)$ by propagating said first conditional carry-out bit, $C_X(1)$ and said second conditional

carry-out bit, $C_X(0)$ through a first pass gate and a second pass gate, respectively, when said first data bit A_{X+1} and said second data bit B_{X+1} are not equal

Independent Claim 23 has been amended to recite receiving a first data bit, A_{X+1}, from the first M-bit argument and a first data bit, B_{X+1}, from the second M-bit argument in the second adder cell, and generating in said second adder cell both a first conditional carry-out bit, $C_{X+1}(1)$, and a second conditional carry-out bit, $C_{X+1}(0)$ by propagating said carry-out bit $C_X(1)$ and said second conditional carry-out bit $C_X(0)$ through a first pass gate and a second pass gate, respectively, when said first data bit A_{X+1} and said second data bit B_{X+1} are not equal.

Uya fails to disclose this element/feature as recited in Applicant's independent claims. Uya's adder cells (as described more particularly in Figures 3 and 4) appear to utilize a series of NAND logic gates 63, 64. 63', 64' (having A, B and Carry inputs). In contrast, Applicant's independent claims recite generating the conditional carry-out bit by propagating the conditional input carry bit through a pass gate (or switch) when the data bits A, B are unequal. As noted in the Applicant's specification, in one embodiment, the time critical data paths through the adder cells in each row are the dual carry paths. See, Specification, page 26, lines 16-20. Applicant utilizes pass gates (or switches) to decrease the delay in these paths. Uya does note disclose the recited elements/features in Applicant's independent claims (as amended).

Accordingly, the Applicant respectfully requests the Examiner withdraw the § 102(b) rejection of Claims 1-23.[1]

II. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

[1] Applicant has also added new dependent Claims 24-31. These claims are allowable as being dependent on allowable independent claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@munckbutrus.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Munck Butrus Deposit Account No. 50-0208.

Respectfully submitted,

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